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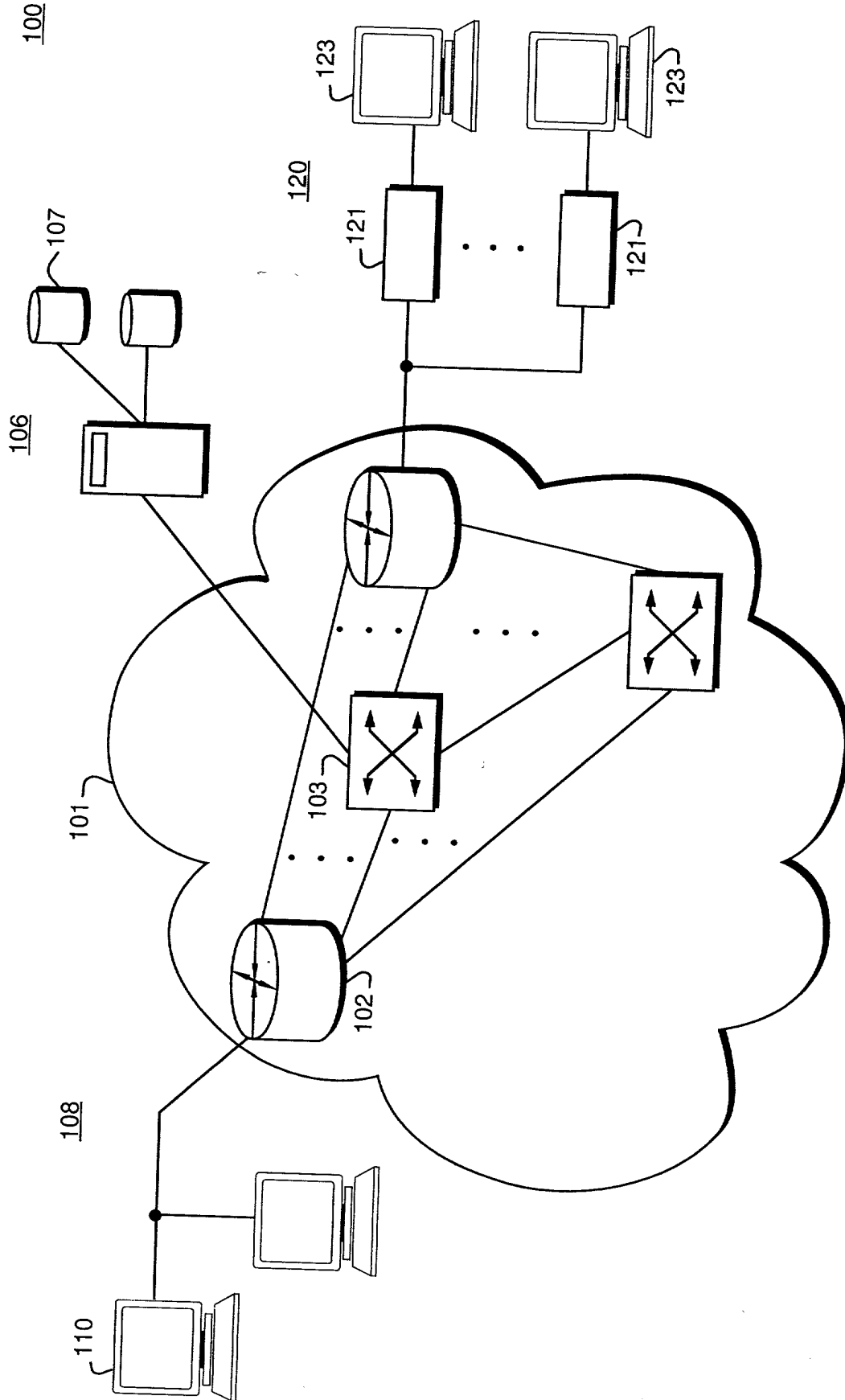


FIG. 1

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102,103

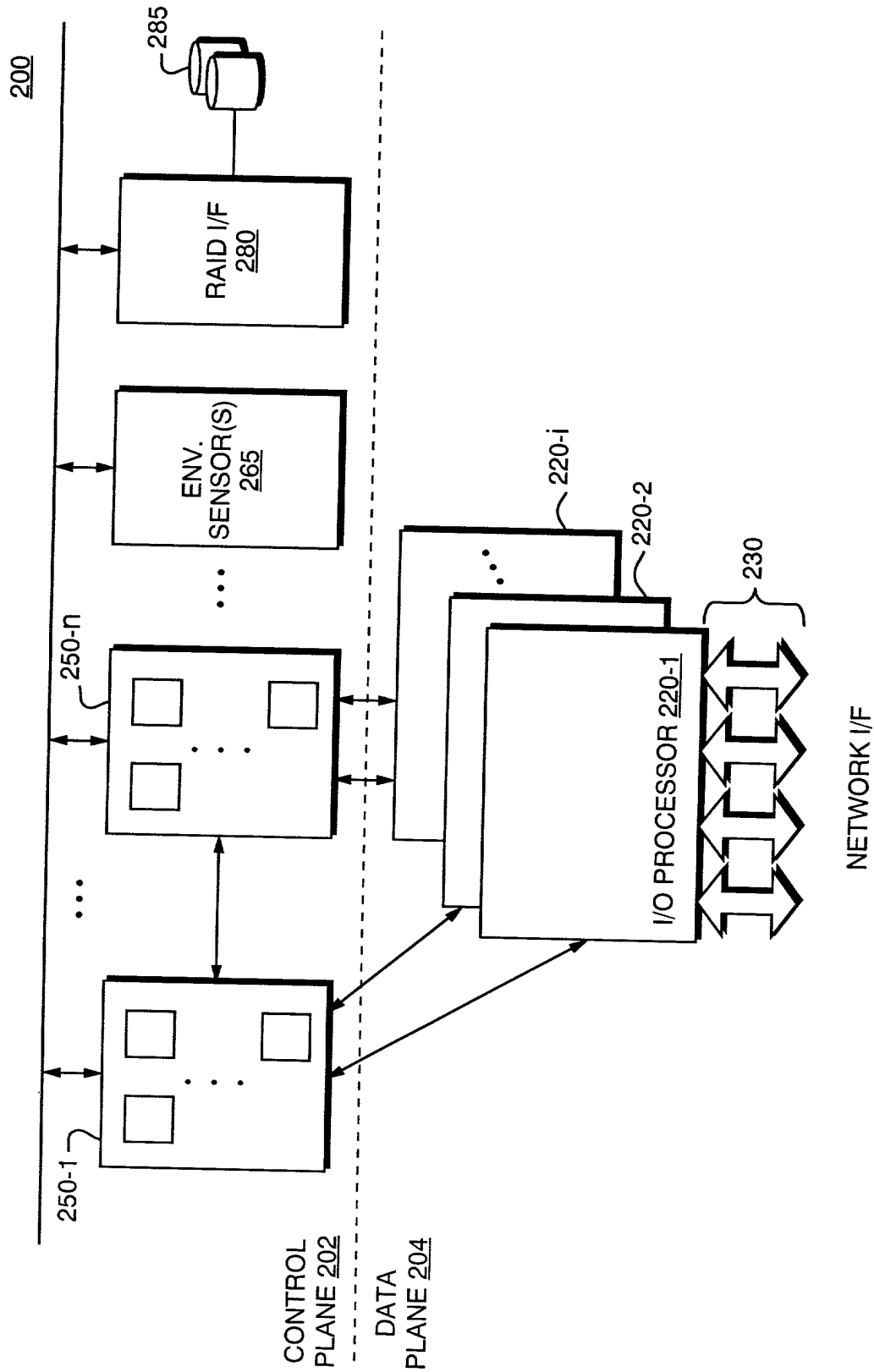


FIG. 2

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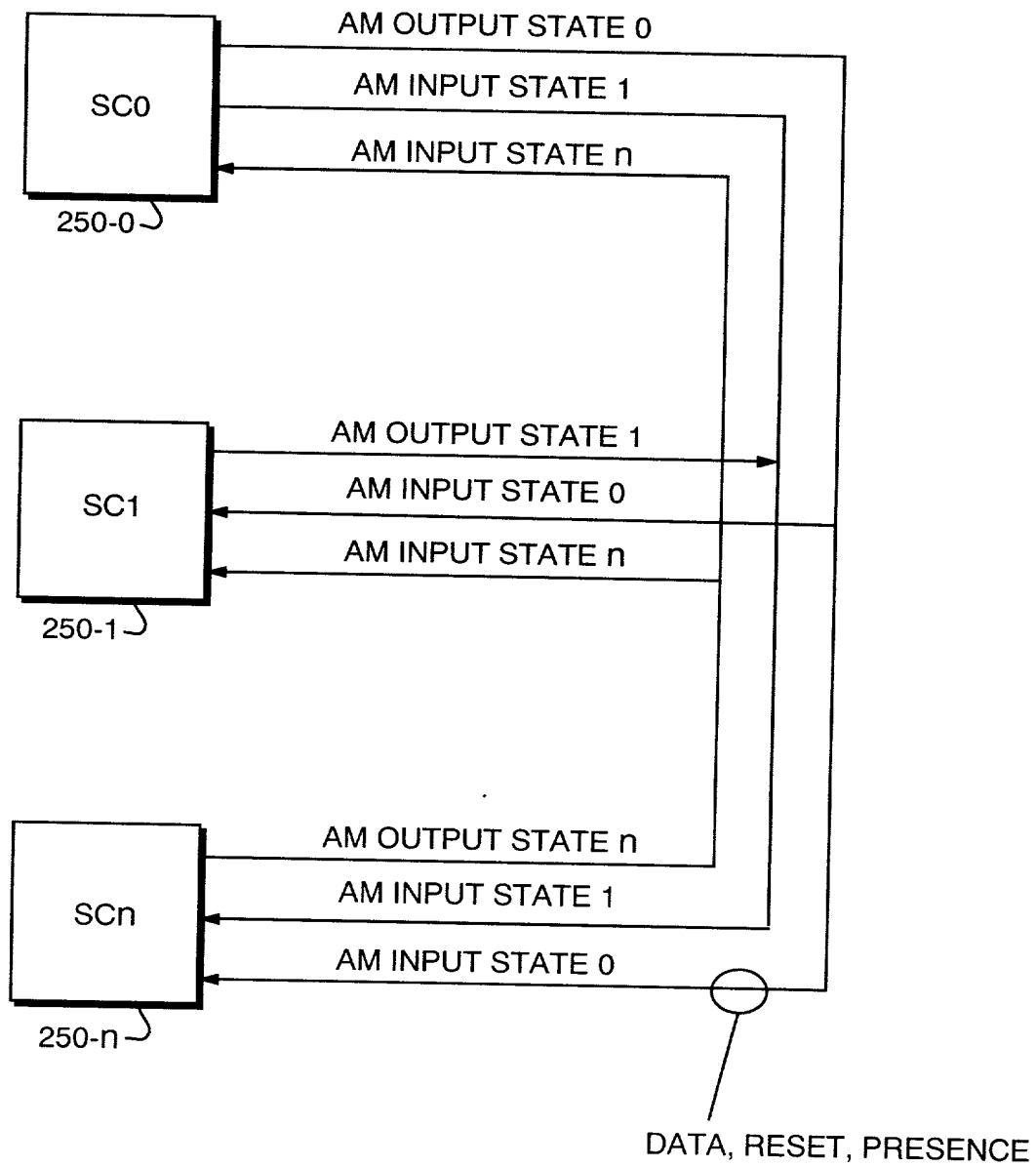


FIG. 3

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# TRANSITIONS

I => P (more than one cpu card is present)

I => C (only one cpu card is present)

P => C (the Pause State duration expired)

C => I (temporary/committed identity conflict encountered)

C => W (identity committed to master-write register)

W => W (wait for event)

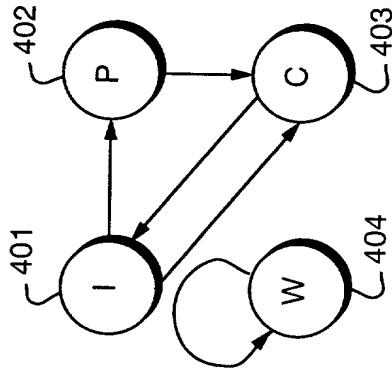


FIG. 4

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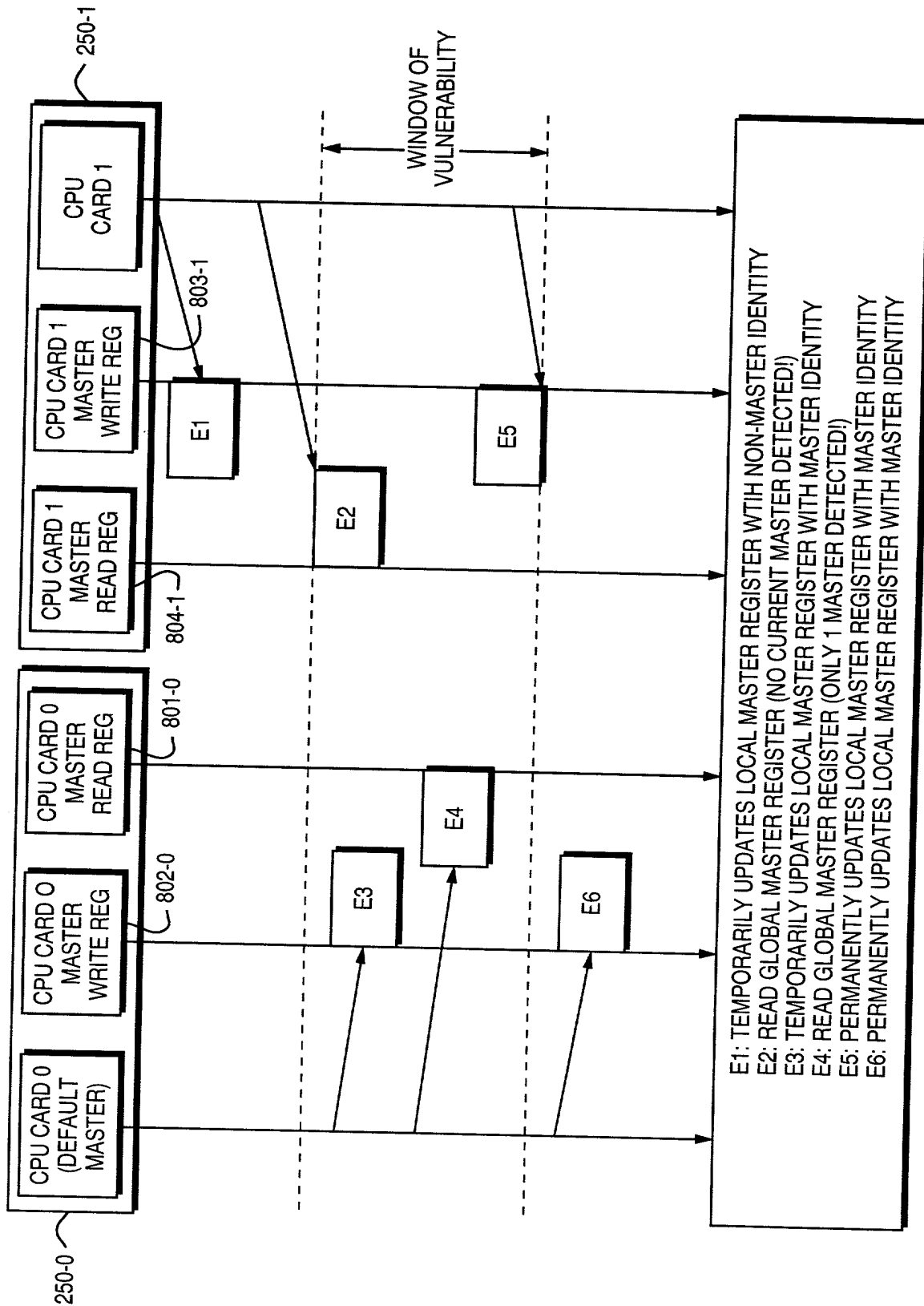


FIG. 5

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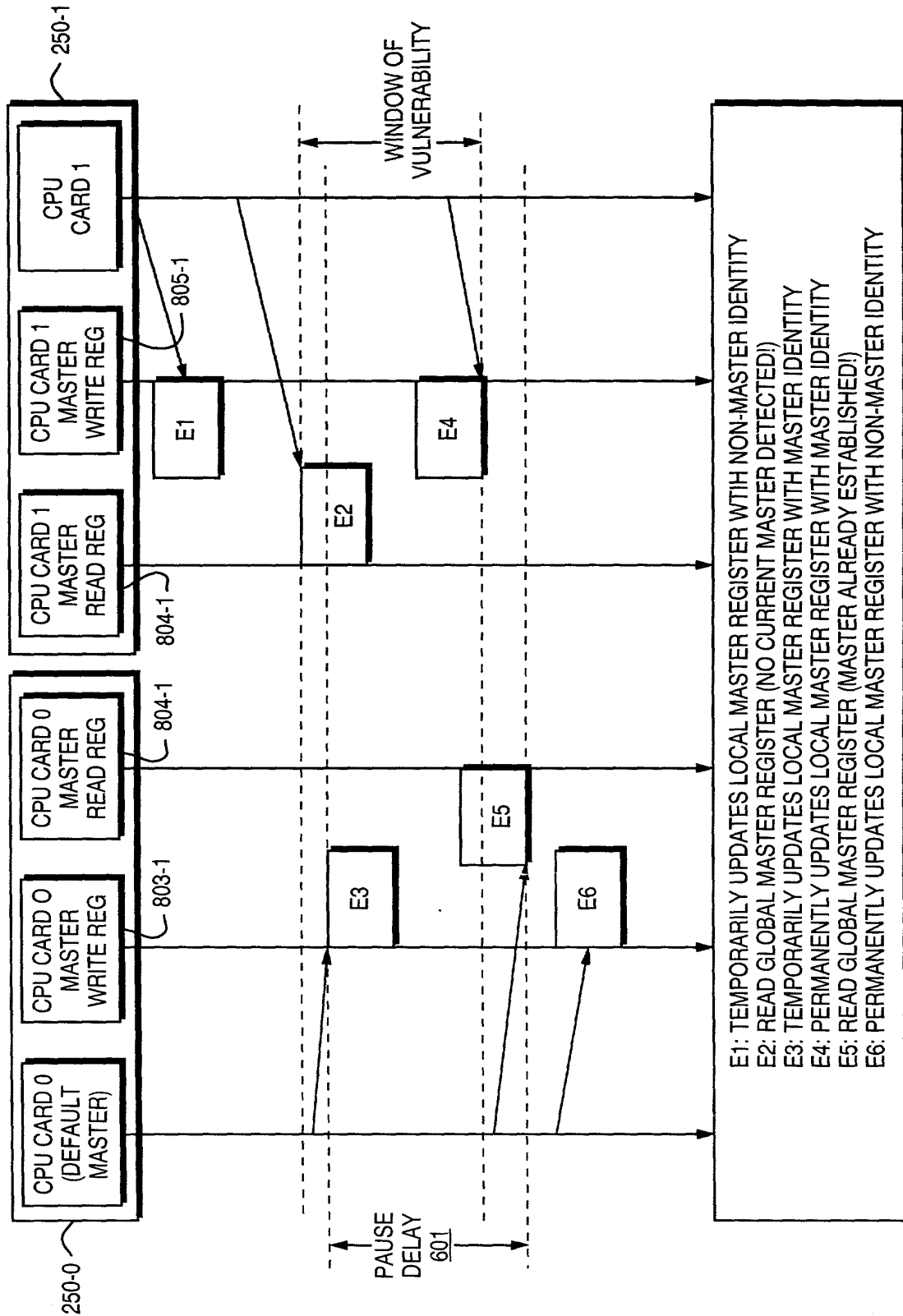


FIG. 6

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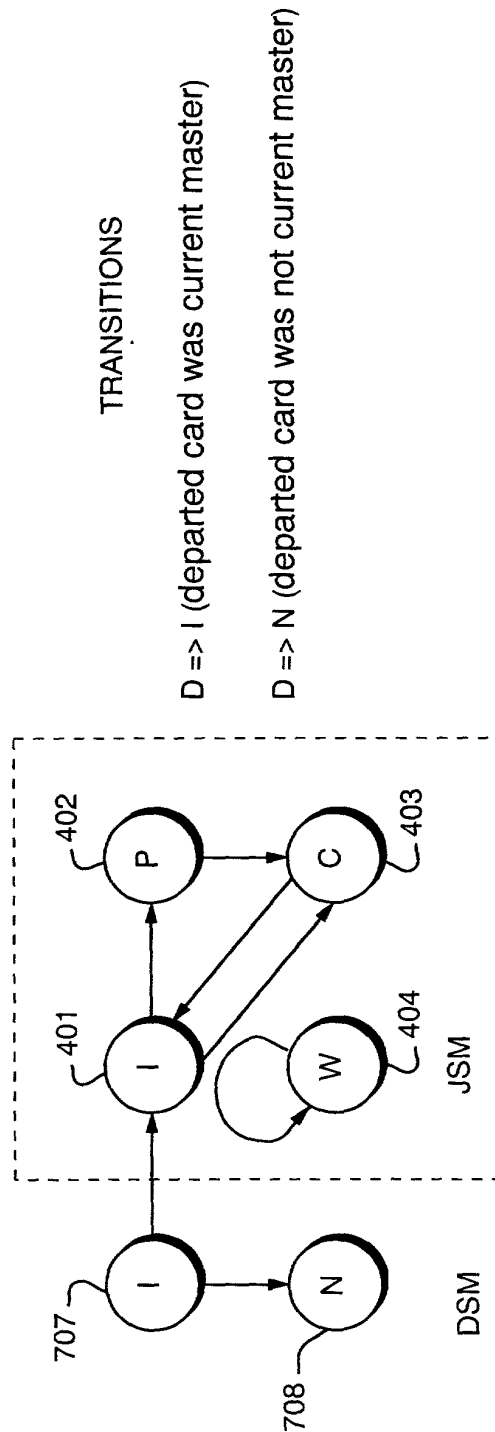


FIG. 7

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801

BIT FIELD	R/W	DEFAULT	FUNCTION
0	R/W	0	SC MASTER STATE
31:2	R/W	0x0000000	RESERVED

FIG. 8A

802

BIT FIELD	R/W	DEFAULT	FUNCTION
0	R	0	SC0 PRESENT
1	R	0	SC1 PRESENT
n	R	0	SCn PRESENT
31:n+1	R	0x0000000	RESERVED

FIG. 8B

803

BIT FIELD	HOST R/W	DEFAULT	FUNCTION
7:0	R/W	0x00	SOFTWARE SPECIFIED
31:8	R	0x000000	RESERVED

FIG. 8C

804

BIT FIELD	HOST R/W	DEFAULT	FUNCTION
7:0	R	0x00	RSC AM STATE (SOFTWARE SPECIFIED)
31:8	R	0x000000	RESERVED

FIG. 8D

805

806

807

BIT FIELD	HOST R/W	DEFAULT	FUNCTION
0	W/R	0x0	AM RECEIVE DATA INTERRUPT
1	R	0x000000	AM RESET INTERRUPT (RSC HAS BEEN RESET)
2	R	0x000000	AAM SLOT CHANGE INTERRUPT (RSC INSERTED OR EXTRACTED)
31:8	R	0x0000000	RESERVED

FIG. 8E

0954711 044660





**FIG. 9**

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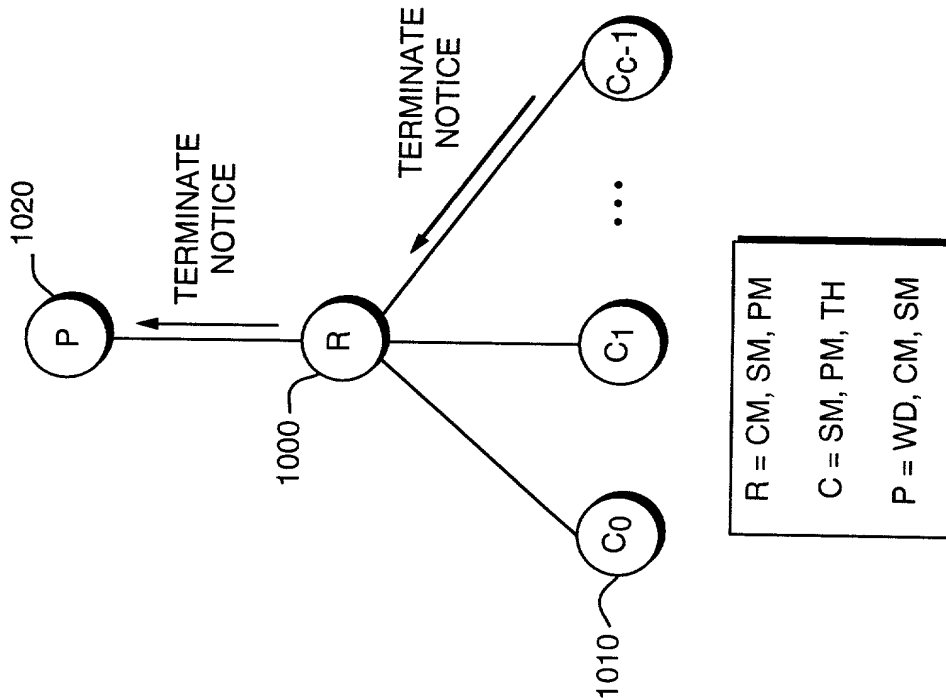


FIG. 10

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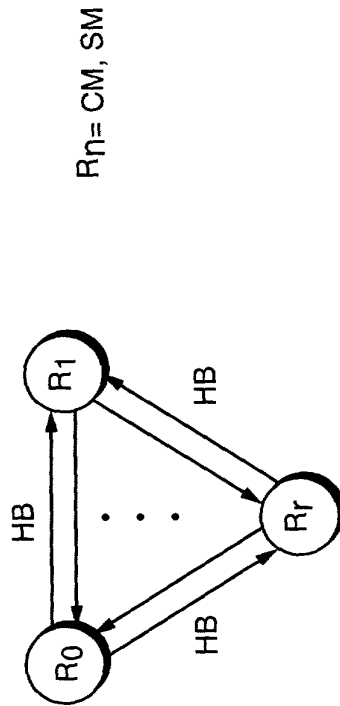


FIG. 11

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